ELECTROLESS PLATING LIQUID AND SEMICONDUCTOR DEVICE

BACKGROUND OF THE INVENTION

Field of the Invention:

This invention relates to an electroless-plating liquid and a semiconductor device. More particularly, this invention relates to an electroless-plating liquid useful for forming a protective film for selectively protecting the surface of the exposed interconnects of a semiconductor device which has such an embedded interconnect structure that an electric conductor, such as copper or silver, is filled in fine recesses for interconnects formed in the surface of a substrate such as a semiconductor substrate, and to a semiconductor device in which the surface of the exposed interconnects is selectively protected with a protective film.

Description of the Related Art:

As a process for forming interconnects in a semiconductor device, the so-called "damascene process", which comprises filling trenches for interconnects and contact holes with a metal (electric conductor), is coming into practical use. According to this process, aluminum or, more recently a metal such as copper or silver, is embedded into trenches for interconnects and contact holes previously formed in the interlevel dielectric of a semiconductor substrate. Thereafter, an extra metal is removed by chemical mechanical polishing (CMP) so as to flatten the surface of the substrate.

In the case of interconnects formed by such a process, the embedded interconnects have an exposed surface after the flattening processing. When an additional embedded interconnect

structure is formed on such an interconnects-exposing surface of a semiconductor substrate, the following problems may be encountered. For example, during the formation of a new SiO_2 at the next interlevel dielectric forming process, the exposed surface of the pre-formed interconnects is likely to be oxidized. Further, upon etching of the SiO_2 layer for formation of via holes, the pre-formed interconnects exposed on the bottoms of the via holes can be contaminated with an etchant, a peeled resist, etc.

In order to avoid such problems, it has conventionally been conducted to form a protective film of SiN or the like not only on the surface region of a semiconductor substrate where the interconnects are exposed, but on the whole surface of the substrate, thereby preventing the contamination of the exposed interconnects with an etchant, etc.

However, the provision of a protective film of SiN or the like on the whole surface of a semiconductor substrate, in a semiconductor device having an embedded interconnect structure, increases the dielectric constant of the interlevel dielectric, thus inducing interconnect delaying even when a low-resistance material such as copper or silver is employed for interconnects, whereby the performance of the semiconductor device may be impaired.

In view of this, it has been proposed to selectively cover the surface of the exposed interconnects to protect the interconnects with an alloy film having a good adhesion to an interconnect material such as copper or silver and having a low resistivity (ρ). The alloy film, for example, is obtained by electroless plating.

The provision of such a protective alloy film by electroless plating, however, has the following problems associated with sodium hypophosphite which is generally used as a reducing agent in electroless plating:

① The inclusion of sodium in the reducing agent can cause the alkali-metal contamination of the semiconductor device.

② When sodium hypophosphite is used as a reducing agent, it is not possible to apply an oxidizing electric current to copper or the like. This necessitates imparting a palladium catalyst to copper or the like, thus increasing the number of process steps and decreasing the throughput.

③ The impartment of a palladium catalyst to copper or the like, in principle, substitutes the underlying interconnects of copper or the like by the palladium, and causes formation of voids in the interconnects, thus lowering the reliability of the interconnects.

④ Since palladium is in the nature of diffusing into copper or the like, the impartment of a palladium catalyst increases the electric resistance of the interconnects.

⑤ Besides on the interconnect formed region, the plated film is likely to be deposited also on the insulating film, making it difficult to perform the intended selective plating.

SUMMARY OF THE INVENTION

The present invention has been made in view of the above drawbacks in the related art. It is therefore an object of the present invention to provide an electroless-plating liquid which can form a plated film (protective film) that selectively covers

only a surface of interconnects and protects the exposed interconnects, without causing any alkali-metal contamination nor formation of voids in interconnects, and to provide a semiconductor device in which the exposed interconnects are selectively protected with a protective film.

In order to achieve the above object, the present invention provides an electroless-plating liquid for selectively forming a plated film on a surface of an exposed interconnect of a semiconductor device having an embedded interconnect structure, the electroless-plating liquid comprising cobalt ions, a complexing agent, and a reducing agent free from alkali metal.

The use of the reducing agent free from alkali metal can prevent contamination of the semiconductor device with an alkali metal.

An alkylamine borane may be used as the reducing agent free from alkali metal. The use of such a reducing agent makes it possible to apply an oxidizing electric current to copper or a copper alloy, or to silver or a silver alloy, thus enabling a direct electroless plating. Further the use of an alkylamine borane, which is free from sodium, can prevent the contamination of the semiconductor device with an alkali metal and, in addition, makes it possible to carry out electroless plating without using a palladium catalyst.

Specific examples of the alkylamine borane may include dimethylamine borane, diethylamine borane and trimethylamine borane.

The electroless-plating liquid may further contain at least one of a stabilizer selected from one or more kinds of heavy metal

compounds and sulfur compounds, and a surfactant.

It is preferred that a pH of the electroless-plating liquid be adjusted within the range from 5 to 14 using a pH adjusting agent free from alkali metal. The use of an alkali metal-free pH adjusting agent, such as ammonia water or quaternary ammonium hydroxide, can keep the plating liquid free from sodium. The plating liquid preferably has a pH from 6 to 10.

The present invention also provides an electroless-plating liquid for selectively forming a plated film on a surface of an exposed interconnect of a semiconductor device having an embedded interconnect structure, the electroless-plating liquid comprising cobalt ions, a complexing agent, a compound containing a refractory metal and a reducing agent free from alkali metal.

At least one of tungsten and molybdenum may be employed as the refractory metal. The reducing agent may be an alkylamine borane. By using such compounds, the electroless-plating liquid provides a protective film of a Co-W-B alloy, a Co-Mo-B alloy or a Co-Mo-W-B alloy to cover the surface of the exposed interconnects.

The present invention also provides a semiconductor device having an embedded interconnect structure of copper, copper alloy, silver or silver alloy interconnect, wherein a surface of an exposed interconnect is selectively covered with a protective film, the protective film being formed by an electroless-plating process with use of an electroless-plating liquid, the electroless-plating liquid comprising cobalt ions, a complexing agent, and a reducing agent free from alkali metal.

By thus selectively covering the surface of the interconnects and protecting the interconnects with the protective

film of an alloy that has a high adhesion to silver or copper and has a low resistivity (ρ), the increase in the dielectric constant of the interlevel dielectric of a semiconductor device having an embedded interconnect structure can be suppressed. Further, the use as an interconnect material of a low-resistance material, such as silver or copper, can attain speedup and densification of the semiconductor.

The present invention also provides a semiconductor device having an embedded interconnect structure, wherein a surface of an exposed interconnect is selectively covered with a protective film of a metal comprising cobalt. The metal film preferably has a thickness within the range from 0.1 to 500 nm.

The present invention further provides a semiconductor device having an embedded interconnect structure, wherein a surface of an exposed interconnect is selectively covered with a protective film of an alloy comprising cobalt and a refractory metal. The refractory metal may preferably be at least one of tungsten and molybdenum.

Examples of the alloy include Co-B alloy, Co-P alloy, Co-W-B alloy, Co-W-P alloy, Co-Mo-B alloy, Co-Mo-P alloy, Co-W-Mo-B alloy, Co-W-Mo-P alloy, Co-Ti-B alloy, Co-Ti-P alloy, Co-Ta-B alloy, Co-Ta-P alloy, Co-Ti-Ta-B alloy, Co-Ti-Ta-P alloy, Co-Ti-W-B alloy, Co-Ti-W-P alloy, Co-Ti-Mo-B alloy, Co-Ti-Mo-P alloy, Co-Ti-Ta-B alloy, Co-Ti-Ta-P alloy, Co-Ta-W-B alloy, Co-Ta-W-P alloy, Co-Ta-Mo-B alloy, Co-Ta-Mo-P alloy, Co-Ti-W-Mo-B alloy, Co-Ti-W-Mo-P alloy, Co-Ta-W-Mo-B alloy, Co-Ta-W-Mo-P alloy, Co-Ti-Ta-W-Mo-B alloy and Co-Ti-Ta-W-Mo-P alloy.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. 1A through 1C illustrate, in a sequence of process steps, an example of forming copper interconnects in a semiconductor device in accordance with the present invention;

FIG. 2 is a schematic view of an example of an electroless-plating device;

FIG. 3 is a schematic view of another example of an electroless-plating device;

FIG. 4 is a plan view of an example of a semiconductor producing apparatus for producing a semiconductor device in accordance with the present invention;

FIG. 5 is a plan view of another example of a semiconductor producing apparatus for producing a semiconductor device in accordance with the present invention;

FIG. 6 is a plan view of yet another example of a semiconductor producing apparatus for producing a semiconductor device in accordance with the present invention;

FIGS. 7A and 7B are diagrams of SEM photographs of the test sample obtained in Example; and

FIGS. 8A and 8B are diagrams of SEM photographs of the test sample obtained in Comparative Example.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Preferred embodiments of the present invention will now be described with reference to the drawings.

FIGS. 1A through 1C illustrate, in a sequence of process steps, an example of forming copper interconnects in a semiconductor device of the present invention. As shown in FIG.

1A, an insulating film 2 of SiO_2 is deposited on a conductive layer 1a formed on a semiconductor base 1 bearing semiconductor devices. A contact hole 3 and a trench 4 for interconnects are formed in the insulating film 2 by the lithography/etching technique. Thereafter, a barrier layer 5 of TaN or the like is formed on the entire surface, and a copper seed layer 6 as an electric supply layer for electroplating is formed on the barrier layer 5 by sputtering or the like.

Then, as shown in FIG. 1B, copper plating is performed onto the surface of the semiconductor substrate W to fill the contact hole 3 and the trench 4 with copper and, at the same time, deposit a copper film 7 on the insulating film 2. Thereafter, the copper film 7 on the insulating layer 2 is removed by chemical mechanical polishing (CMP) so as to make the surface of the copper film 7 filled in the contact hole 3 and the trench 4 for interconnects and the surface of the insulating film 2 lie substantially on the same plane. Interconnects 8 composed of the copper seed layer 6 and the copper film 7, as shown in FIG. 1C, are thus formed in the insulating layer 2.

Next, electroless plating is performed onto the surface of the semiconductor substrate W to selectively form a protective film 9 composed of an alloy film on the exposed surface of the interconnects 8, thereby protecting the interconnects 8. The thickness of the protective film 9 is generally 0.1-500 nm, preferably 1-200 nm, more preferably 10-100 nm.

The protective film 9 is formed, for example, by using a plating liquid containing cobalt ions, a complexing agent, a pH buffer, a pH adjusting agent and an alkylamine borane as a reducing

agent, or a plating liquid further containing a refractory (high-melting point) metal such as tungsten and molybdenum, and dipping the surface of the semiconductor substrate W in the plating liquid.

If desired, the plating liquid may further contain at least one of a stabilizer selected from one or more kinds of heavy metal compounds and sulfur compounds, and surfactant. Further, the plating liquid is adjusted within a pH range of preferably 5-14, more preferably 6-10, by using a pH adjusting agent such as ammonia water or quaternary ammonium hydroxide. The temperature of the plating liquid is generally in the range of 30-90℃, preferably 40-80℃.

The protection of the interconnects 8 by the provision of the protective film 9 can prevent, in forming thereon an additional embedded interconnect structure, the oxidation of the surface of the interconnect during the formation of a new SiO_2 at the next interlevel dielectric forming process and the contamination of the interconnect with an etchant, a peeled resist or the like upon etching of the SiO_2 layer.

The use of the plating liquid containing cobalt ions, a complexing agent, a pH buffer, a pH adjusting agent and an alkylamine borane as a reducing agent, provides a protective film 9 of a Co-B alloy film. The use of the plating liquid further containing a refractory metal, such as tungsten and molybdenum, provides a protective film 9 of a Co-W-B alloy film, Co-Mo-B alloy film or Co-Mo-W-B alloy film.

By selectively covering the surface of the interconnects 8 and protecting the interconnects 8 with the protective film 9 of

such an alloy film that has a high adhesion to copper as an interconnect material and has a low resistivity (ρ), the increase in the dielectric constant of the interlevel dielectric of a semiconductor device having an embedded interconnect structure can be suppressed. Further, the use of copper as an interconnect material, which is a low-resistance material, can attain speedup and densification of the semiconductor.

Though this example shows the use of copper as an interconnect material, a copper alloy, silver or a silver alloy may also be used.

The cobalt ions contained in the plating liquid may be supplied from a cobalt salt, for example, cobalt sulfate, cobalt chloride or cobalt acetate. The amount of the cobalt ions is generally in the range of 0.001-1 mol/L, preferably 0.01-0.3 mol/L.

Specific examples of the complexing agent may include carboxylic acids, such as acetic acid, or their salts; oxycarboxylic acids, such as tartaric acid and citric acid, and their salts; and aminocarboxylic acids, such as glycine, and their salts. These compounds may be used either singly or as a mixture of two or more. The total amount of the complexing agent is generally 0.001-1.5 mol/L, preferably 0.01-1.0 mol/L.

Regarding the pH buffer, any buffer may be used that does not contain sodium or any other alkali metal. Ammonium sulfate, ammonium chloride and boric acid may be mentioned as specific examples. The pH buffer can be used generally in an amount of 0.01-1.5 mol/L, preferably 0.1-1 mol/L.

Regarding the pH adjusting agent, any agent may be used that does not contain sodium or any other alkali metal. Ammonia water

and tetramethylammonium hydroxide (TMAH) may be mentioned as specific examples. By using the pH adjusting agent, the pH of the plating liquid is adjusted generally within the range of 5-14, preferably 6-10.

The reducing agent likewise should not contain sodium or any other alkali metal. An alkylamine borane is preferably used. As alkylamine boranes, dimethylamine borane (DMAB) and diethylamine borane, may be mentioned. The reducing agent is used generally in an amount of 0.01-1 mol/L, preferably 0.01-0.5 mol/L.

Examples of the compound containing a refractory metal may include tangstic acid, molybdic acid and their salts; and heteropoly acids, such as tangstophosphoric acid (e.g. $H_3(PW_{12}P_{40}) \cdot nH_2O$), and their salts. Ti or Ta may also be used when the formation of the protective film is not by electroless plating. The compound containing a refractory metal point is used generally in an amount of 0.001-1 mol/L, preferably 0.01-0.1 mol/L. Examples of cobalt/refractory metal alloys include Co-B alloy, Co-P alloy, Co-W-B alloy, Co-W-P alloy, Co-Mo-B alloy, Co-Mo-P alloy, Co-W-Mo-B alloy, Co-W-Mo-P alloy, Co-Ti-B alloy, Co-Ti-P alloy, Co-Ta-B alloy, Co-Ta-P alloy, Co-Ti-Ta-B alloy, Co-Ti-Ta-P alloy, Co-Ti-W-B alloy, Co-Ti-W-P alloy, Co-Ti-Mo-B alloy, Co-Ti-Mo-P alloy, Co-Ti-Ta-B alloy, Co-Ti-Ta-P alloy, Co-Ta-W-B alloy, Co-Ta-W-P alloy, Co-Ta-Mo-B alloy, Co-Ta-Mo-P alloy, Co-Ti-W-Mo-B alloy, Co-Ti-W-Mo-P alloy, Co-Ta-W-Mo-B alloy, Co-Ta-W-Mo-P alloy, Co-Ti-Ta-W-Mo-B alloy and Co-Ti-Ta-W-Mo-P alloy. Of these, alloys containing tungsten and/or molybdenum are especially preferred for use in the electroless plating according to the present invention. Alloys containing boran or phosphor are usable insofar as they

contain no alkali metal. Alloys containing Ti or Ta may be used in a process other than electroless plating.

Besides the above described compounds, other known additives may be added to the plating liquid. Examples of usable additive include a bath stabilizer, which may be a heavy metal compound such as a lead compound, a sulfur compound such as a thiocyanate, or a mixture thereof, and a surfactant of an anionic, cationic or nonionic type.

As described above, it is preferred to use as a reducing agent an alkylamine borane free from sodium. The use of an alkylamine borone makes it possible to apply an oxidizing current to copper, a copper alloy, silver, or a silver alloy to thereby avoid the need for imparting a palladium catalyst, thus enabling a direct electroless plating, and can prevent contamination of the semiconductor device with an alkali metal. Thus, the electroless-plating liquid, which utilizes an alkylamine borane as a reducing agent, makes it possible to carry out electroless plating by immersing the surface of the semiconductor device W in the plating liquid, without imparting a palladium catalyst. This can reduce the requisite process steps and increase the throughput, prevent the formation of voids in the copper interconnects caused by palladium replacement and avoid the increase in interconnect resistance caused by palladium diffusion.

Further, it has been found that when electroless plating is performed by using the plating liquid containing the alkylamine borane as the reducing agent, the plating film is deposited selectively on copper or silver. This enables a selective plating only onto the interconnect region.

FIG. 2 is a schematic constitution drawing of the electroless plating apparatus. As shown in FIG. 2, this electroless plating apparatus comprises holding means 11 for holding a semiconductor substrate W on its upper surface, a dam member (plating liquid holding mechanism) 31 for contacting a peripheral edge portion of a surface to be plated (upper surface) of the semiconductor substrate W held by the holding means 11 to seal the peripheral edge portion, and a shower head (an electroless plating liquid (scattering) supply means) 41 for supplying a plating liquid (an electroless plating liquid) to the surface, to be plated, of the semiconductor substrate W having the peripheral edge portion sealed with the dam member 31. The electroless plating apparatus further comprises cleaning liquid supply means 51 disposed near an upper outer periphery of the holding means 11 for supplying a cleaning liquid to the surface, to be plated, of the semiconductor substrate W, a recovery vessel 61 for recovering a cleaning liquid or the like (plating waste liquid) discharged, a plating liquid recovery nozzle 65 for sucking in and recovering the plating liquid held on the semiconductor substrate W, and a motor (rotational drive means) M for rotationally driving the holding means 11.

The holding means 11 has a substrate placing portion 13 on its upper surface for placing and holding the semiconductor substrate W. The substrate placing portion 13 is adapted to place and fix the semiconductor substrate W. Specifically, the substrate placing portion 13 has a vacuum attracting mechanism (not shown) for attracting the semiconductor substrate W on a backside thereof by vacuum suction. A backside heater (heating means) 15, which is planar and heats the surface, to be plated, of the

semiconductor substrate W from underside to keep it warm, is installed on the backside of the substrate placing portion 13. The backside heater 15 is composed of, for example, a rubber heater. This holding means 11 is adapted to be rotated by the motor M and is movable vertically by lifting means (not shown).

The dam member 31 is tubular, has a seal portion 33 provided in a lower portion thereof for sealing the outer peripheral edge of the semiconductor substrate W, and is installed so as not to move vertically from the illustrated position.

The shower head 41 is of a structure having many nozzles provided at the front end for scattering the supplied plating liquid in a shower form and supplying it substantially uniformly to the surface, to be plated, of the semiconductor substrate W. The cleaning liquid supply means 51 has a structure for ejecting a cleaning liquid from a nozzle 53.

The plating liquid recovery nozzle 65 is adapted to be movable upward and downward and swingable, and the front end of the plating liquid recovery nozzle 65 is adapted to be lowered inwardly of the dam member 31 located on the upper surface peripheral edge portion of the semiconductor substrate W and to suck in the plating liquid on the semiconductor substrate W.

Next, the operation of the electroless plating apparatus will be described. First, the holding means 11 is lowered from the illustrated state to provide a gap of a predetermined dimension between the holding means 11 and the dam member 31, and the semiconductor substrate W is placed on and fixed to the substrate placing portion 13. An 8 inch wafer, for example, is used as the semiconductor substrate W.

Then, the holding means 11 is raised to bring its upper surface into contact with the lower surface of the dam member 31 as illustrated in FIG. 2, and the outer periphery of the semiconductor substrate W is sealed with the seal portion 33 of the dam member 31. At this time, the surface of the semiconductor substrate W is in an open state.

Then, the semiconductor substrate W itself is directly heated by the backside heater 15, while the plating liquid is ejected from the shower head 41 to pour the plating liquid over substantially the entire surface of the semiconductor substrate W. Since the surface of the semiconductor substrate W is surrounded by the dam member 31, the poured plating liquid is all held on the surface of the semiconductor substrate W. The amount of the supplied plating liquid may be a small amount which will become a 1 mm thickness (about 30 ml) on the surface of the semiconductor substrate W. The depth of the plating liquid held on the surface to be plated may be 10 mm or less, and may be even 1 mm as in this embodiment. If a small amount of the supplied plating liquid is sufficient, the heating apparatus for heating the plating liquid may be of a small size.

If the semiconductor substrate W itself is adapted to be heated, the temperature of the plating liquid requiring great power consumption for heating need not be raised so high. This is preferred, because power consumption can be decreased, and a change in the property of the plating liquid can be prevented. Power consumption for heating of the semiconductor substrate W itself may be small, and the amount of the plating liquid stored on the semiconductor substrate W is also small. Thus, heat retention of

the semiconductor substrate W by the backside heater 15 can be performed easily, and the capacity of the backside heater 15 may be small, and the apparatus can be made compact. If means for directly cooling the semiconductor substrate W itself is used, switching between heating and cooling may be performed during plating to change the plating conditions. Since the plating liquid held on the semiconductor substrate is in a small amount, temperature control can be performed with good sensitivity.

The semiconductor substrate W is instantaneously rotated by the motor M to perform uniform liquid wetting of the surface to be plated, and then plating of the surface to be plated is performed in such a state that the semiconductor substrate W is in a stationary state. Specifically, the semiconductor substrate W is rotated at 100 rpm or less for only 1 second to uniformly wet the surface, to be plated, of the semiconductor substrate W with the plating liquid. Then, the semiconductor substrate W is kept stationary, and electroless plating is performed for 1 minute. The instantaneous rotating time is 10 seconds or less at the longest.

After completion of the plating treatment, the front end of the plating liquid recovery nozzle 65 is lowered to an area near the inside of the dam member 31 on the peripheral edge portion of the semiconductor substrate W to suck in the plating liquid. At this time, if the semiconductor substrate W is rotated at a rotational speed of, for example, 100 rpm or less, the plating liquid remaining on the semiconductor substrate W can be gathered in the portion of the dam member 31 on the peripheral edge portion of the semiconductor substrate W under centrifugal force, so that recovery of the plating liquid can be performed with a good

efficiency and a high recovery rate. The holding means 11 is lowered to separate the semiconductor substrate W from the dam member 31. The semiconductor substrate W is started to be rotated, and the cleaning liquid (ultrapure water) is jetted at the plated surface of the semiconductor substrate W from the nozzle 53 of the cleaning liquid supply means 51 to cool the plated surface, and simultaneously perform dilution and cleaning, thereby stopping the electroless plating reaction. At this time, the cleaning liquid jetted from the nozzle 53 may be supplied to the dam member 31 to perform cleaning of the dam member 31 at the same time. The plating waste liquid at this time is recovered into the recovery vessel 61 and discarded.

The plating liquid once used is not reused, but thrown away. As stated above, the amount of the plating liquid used in this apparatus can be made very small, compared with that in the prior art. Thus, the amount of the plating liquid which is discarded is small, even without reuse. In some cases, the plating liquid recovery nozzle 65 may not be installed, and the plating liquid which has been used may be recovered as a plating waste liquid into the recovery vessel 61, together with the cleaning liquid.

Then, the semiconductor substrate W is rotated at a high speed by the motor M for spin-drying, and then the semiconductor substrate W is removed from the holding means 11.

FIG. 3 is a schematic constitution drawing of an another electroless plating apparatus. The embodiment of FIG. 3 is different from the aforementioned elecroless plating apparatus shown in FIG. 2 in that instead of providing the backside heater 15 in the holding means 11, lamp heaters (heating means) 17 are

disposed above the holding means 11, and the lamp heaters 17 and a shower head 41-2 are integrated. For example, a plurality of ring-shaped lamp heaters 17 having different radii are provided concentrically, and many nozzles 43-2 of the shower head 41-2 are open in a ring form from the gaps between the lamp heaters 17. The lamp heaters 17 may be composed of a single spiral lamp heater, or may be composed of other lamp heaters of various structures and arrangements.

Even with this constitution, the plating liquid can be supplied from each nozzle 43-2 to the surface, to be plated, of the semiconductor substrate W substantially uniformly in a shower form. Further, heating and heat retention of the semiconductor substrate W can be performed by the lamp heaters 17 directly uniformly. The lamp heaters 17 heat not only the semiconductor substrate W and the plating liquid, but also ambient air, thus exhibiting a heat retention effect on the semiconductor substrate W.

Direct heating of the semiconductor substrate W by the lamp heaters 17 requires the lamp heaters 17 with relatively large power consumption. In place of such lamp heaters 17, lamp heaters 17 with relatively small power consumption and the backside heater 15 shown in FIG. 2 may be used in combination to heat the semiconductor substrate W mainly with the backside heater 15 and to perform heat retention of the plating liquid and ambient air mainly by the lamp heaters 17. In the same manner as in the aforementioned embodiment, means for directly or indirectly cooling the semiconductor substrate W may be provided to perform temperature control.

FIG. 4 is a plan view of an example of an semiconductor producing apparatus for producing a semiconductor device in accordance with the present invention. The semiconductor producing apparatus includes a loading/unloading section 201 housing a cassette 201-1, a first plating device 202, a first robot 203, reversing devices 205 and 206, a second cleaning device 207, a second robot 208, a first cleaning device 209, a second plating device 227, a first polishing device 210 and a second polishing device 211. Further, in the vicinity of the first robot 203, a before/after plating-film thickness-measuring device 212 for measuring the thickness of a plated film before and after plating, and a dry state film thickness-measuring device 213 for measuring the thickness of a dry-state film on the semiconductor substrate W after polishing, are provided.

The first polishing device 210 has a polishing table 210-1, a top ring 210-2, a top ring head 210-3, a film thickness-measuring device 210-4 and a pusher 210-5. The second polishing device 211 has a polishing table 211-1, a top ring 211-2, a top ring head 211-3, a film thickness-measuring device 211-4 and a pusher 211-5.

The process steps in the apparatus will now be described.

First, the cassette 201-1 housing semiconductor substrates W, on each of which a copper seed layer 6 (see FIG.1A) is formed, is placed on a loading port in the loading/unloading section 201. The semiconductor substrate is taken out by the first robot 203, and a copper film 7 (see FIG. 1B) is formed by the first plating device 202. Formation of the copper film 7 is performed by carrying out hydrophilic treatment of the face of the semiconductor substrate W, and then copper plating. Then, rinsing or cleaning

is carried out. If there is some time to spare, drying may be performed. When the semiconductor substrate W is taken out by the first robot 203, the film thickness of the plated copper film 7 is measured with the before-plating and after-plating film thickness measuring instrument 212. The results of the measurement are recorded as record data on the semiconductor substrate W and are also used for judgment of an abnormality of the first plating device 202. After measurement of the film thickness, the first robot 203 transfers the semiconductor substrate W to a reversing device 205 in which the semiconductor substrate W is turned over.

Then, a second robot 208 picks up the semiconductor substrate W from the reversing device 205, and places it on a pusher 210-5 or 211-5. Then, the top ring 210-2 or 211-2 holds the semiconductor substrate W by suction, transfers it onto a polishing table 210-1 or 211-1, and presses it against a polishing surface on the polishing table 210-1 or 211-1 to perform polishing.

After completion of polishing, the top ring 210-2 or 211-2 returns the semiconductor substrate W to the pusher 210-5 or 211-5. The second robot 208 picks up the semiconductor substrate W, and carries it into a first cleaning device 209. At this time, a chemical liquid may be ejected toward the face and backside of the semiconductor substrate W on the pusher 210-5 or 211-5 to remove particles therefrom or cause particles to be difficult to adhere thereto.

In the first cleaning device 209, the face and the backside of the semiconductor substrate W are scrubbed and cleaned. The face of the semiconductor substrate W is scrubbed and cleaned mainly

for removal of particles with a PVA roll sponge using cleaning water comprising pure water to which a surface active agent, a chelating agent, or a pH adjusting agent is added. A strong chemical liquid such as DHF is ejected toward the backside of the semiconductor substrate W to etch diffused copper. If there is no problem of copper diffusion, the backside of the semiconductor substrate W is scrubbed and cleaned with a PVA roll sponge using the same chemical liquid as that for the face.

After the cleaning, the second robot 208 picks up the semiconductor substrate W, and transfers it to the reversing device 206 where the semiconductor substrate W is reversed. The second robot 208 again picks up the semiconductor substrate W and transport it to the second plating device 227 which is constituted, for example, by the electroless-plating device as shown in FIG. 2 or FIG. 3. In the second plating device 227, the surface of the semiconductor substrate W is immersed in a plating liquid, e.g. the above described electroless-plating liquid, and the protective film 9 of an alloy is selectively formed on the exposed surface of the interconnects 8 to protect the interconnects 8 (see FIG. 1C). Thereafter, the second robot 208 picks up the semiconductor substrate W, transfers it to the reversing device 206, where the semiconductor substrate W is reversed, and then transfers the substrate to the second cleaning device 207. In the second cleaning device 207, megasonic water to which ultrasonic vibrations are applied is ejected toward the face of the semiconductor substrate W to clean the face. At this time, the face may be cleaned with a pencil type sponge using a cleaning liquid comprising pure water to which a surface active agent, a chelating

agent, or a pH adjusting agent is added. Thereafter, the semiconductor substrate W is dried by spin-drying.

Then, the second robot 208 picks up the semiconductor substrate W, and transfers it to the reversing device 206 as it is. The first robot 203 picks up the semiconductor substrate W on the reversing device 206. In the case where the film thickness has been measured with a film thickness measuring instrument 210-4 or 211-4 provided near the polishing table 210-1 or 211-1, the semiconductor substrate W is received by the cassette 201-1 placed in the unload port of the loading/unloading section 201. In the case where the film thicknesses of multilayer films are to be measured, measurement in a dry state needs to be performed. Thus, the film thickness is measured once with a dry state film thickness measuring instrument 213.

FIG. 5 is a plan view of another example of a semiconductor producing apparatus for producing a semiconductor device in accordance with the present invention. As with the substrate-processing apparatus of FIG. 4, this semiconductor producing apparatus performs the substrate processing comprising the steps of forming the copper film 6 on the semiconductor substrate W having thereon the seed layer 7, polishing the substrate, and selectively forming the protective film 9 on the interconnects 8, thereby providing a circuit interconnection in which the interconnects 8 are selectively protected with the protective film 9.

In the present semiconductor producing apparatus, a pusher indexer 225 is disposed close to a first polishing apparatus 210 and a second polishing apparatus 211, substrate placing tables 221, 222 are disposed close to a second cleaning device 207 and a second

plating device 227, respectively, and a robot 223 (hereinafter referred to as second robot 223) is disposed close to the second plating device 227 and a first plating device 202. Further, a robot 224 (hereinafter referred to as third robot 224) is disposed close to a first cleaning device 209 and the second cleaning device 207, and a dry state film thickness measuring instrument 213 is disposed close to a loading/unloading section 201 and a first robot 203.

The first robot 203 takes out a semiconductor substrate W having a seed layer 6 thereon from a cassette 201-1 placed on the load port of the loading/unloading section 201, and places it on the substrate placing table 221. Then, the second robot 223 transports the semiconductor substrate W to the first plating device 202 where a copper film 7 (see FIG. 1B) is formed. The second robot 223 transfers the semiconductor substrate having the copper film 7 formed thereon to be measured in thickness of the copper film 7 by the before-plating and after-plating film thickness measuring instrument 212. After measurement of the film thickness, the semiconductor substrate is carried into the pusher indexer 225.

A top ring 210-2 or 211-2 holds the semiconductor substrate W on the pusher indexer 225 by suction, and transfers it to a polishing table 210-1 or 211-1 to perform polishing. After polishing, the top ring 210-2 or 211-2 transfers the semiconductor substrate W to a film thickness measuring instrument 210-4 or 211-4 to measure the film thickness. Then, the top ring 210-2 or 211-2 transfers the semiconductor substrate W to the pusher indexer 225, and places it thereon.

Then, the third robot 224 picks up the semiconductor substrate W from the pushed indexer 225, and carries it into the

first cleaning device 209. After the cleaning in the first cleaning unit 209, the third robot 224 picks up the cleaned semiconductor substrate W, and carries it into the second plating device 227 where the protective film 9 is selectively formed on the surface of the interconnects 8 by e.g. electroless plating, thereby protecting the interconnects 8 (see FIG. 1C). Thereafter, the third robot 224 carries the semiconductor substrate W into the second cleaning device 207 for cleaning and drying, and places the cleaned semiconductor substrate W on the substrate placing table 222. Next, the first robot 203 picks up the semiconductor substrate W and carries it into the dry state film thickness-measuring instrument 213 where the film thickness is measured, and then puts the substrate into the cassette 201-1 placed on the unload port in the loading/unloading section 201.

FIG. 6 is a plan view of yet another example of a semoconductor producing apparatus for producing a semiconductor device in according with the present invention. In the present semiconductor producing apparatus, there are provided a barrier layer forming unit 111, a seed layer forming unit 112, a plated film forming unit 113, an annealing unit 114, a first cleaning unit 115, a bevel and backside cleaning unit 116, a cap plating unit 117 having e.g. electroless-plating device shown in FIG. 2 or FIG. 3, a second cleaning unit 118, a first aligner and film thickness measuring instrument 141, a second aligner and film thickness measuring instrument 142, a first substrate reversing device 143, a second substrate reversing device 144, a substrate temporary placing table 145, a third film thickness measuring instrument 146, a loading/unloading unit 120, a first polishing apparatus 121, a

second polishing apparatus 122, a first robot 131, a second robot 132, a third robot 133, and a fourth robot 134. The film thickness measuring instruments 141, 142, and 146 are units, have the same size as the frontage dimension of other units (plating, cleaning, annealing units, and the like), and are thus interchangeable.

In this embodiment, an electroless Ru plating apparatus can be used as the barrier layer forming unit 111, an electroless copper plating apparatus as the seed layer forming unit 112, and an electroplating apparatus as the plated film forming unit 113.

The process steps in this apparatus will now be described.

First, a semiconductor substrate taken out by the first robot 131 from a cassette 120a placed on the loading/unloading unit 120 is placed in the first aligner and film thickness measuring unit 141, in such a state that its surface, to be plated, faces upward. In order to set a reference point for a position at which film thickness measurement is made, notch alignment for film thickness measurement is performed, and then film thickness data on the semiconductor substrate before formation of a copper film are obtained.

Then, the semiconductor substrate is transported to the barrier layer forming unit 111 by the first robot 131. The barrier layer forming unit 111 is such an apparatus for forming a barrier layer on the semiconductor substrate by electroless Ru plating, and the barrier layer forming unit 111 forms an Ru film as a film for preventing copper from diffusing into an interlayer insulator film (e.g. SiO_2) of a semiconductor device. The semiconductor substrate discharged after cleaning and drying steps is transported by the first robot 131 to the first aligner and film

thickness measuring unit 141, where the film thickness of the semiconductor substrate, i.e., the film thickness of the barrier layer is measured.

The semiconductor substrate after film thickness measurement is carried into the seed layer forming unit 112 by the second robot 132, and a seed layer 6 (see FIG. 1A) is formed on the barrier layer by electroless Cu plating. The semiconductor substrate discharged after cleaning and drying steps is transported by the second robot 132 to the second aligner and film thickness measuring instrument 142 for determination of a notch position, before the semiconductor substrate is transported to the plated film forming unit 113, and then notch alignment for copper plating is performed. If necessary, the film thickness of the semiconductor substrate before formation of a copper film may be measured again in the film thickness measuring instrument 142.

The semiconductor substrate which has completed notch alignment is transported by the third robot 133 to the plated film forming unit 113 where copper plating is applied to the semiconductor substrate. The semiconductor substrate discharged after cleaning and drying steps is transported by the third robot 133 to the bevel and backside cleaning unit 116 where an unnecessary copper film (seed layer) at a peripheral portion of the semiconductor substrate is removed. In the bevel and backside cleaning unit 116, the bevel is etched in a preset time, and copper adhering to the backside of the semiconductor substrate is cleaned with a chemical liquid such as hydrofluoric acid. At this time, before transporting the semiconductor substrate to the bevel and backside cleaning unit 116, film thickness measurement of the

semiconductor substrate may be made by the second aligner and film thickness measuring instrument 142 to obtain the thickness value of the copper film formed by plating, and based on the obtained results, the bevel etching time may be changed arbitrarily to carry out etching. The region etched by bevel etching is a region which corresponds to a peripheral edge portion of the substrate and has no circuit formed therein, or a region which is not utilized finally as a chip although a circuit is formed. A bevel portion is included in this region.

The semiconductor substrate discharged after cleaning and drying steps in the bevel and backside cleaning unit 116 is transported by the third robot 133 to the substrate reversing device 143. After the semiconductor substrate is turned over by the substrate reversing device 143 to cause the plated surface to be directed downward, the semiconductor substrate is introduced into the annealing unit 114 by the fourth robot 134 for thereby stabilizing an interconnect portion. Before and/or after annealing treatment, the semiconductor substrate is carried into the second aligner and film thickness measuring unit 142 where the film thickness of a copper film 7 (see FIG. 1B) formed on the semiconductor substrate is measured. Then, the semiconductor substrate is carried by the fourth robot 134 into the first polishing apparatus 121 in which the copper film 7 and the seed layer 6 (see FIG. 1A) of the semiconductor substrate are polished.

At this time, desired abrasive grains or the like are used, but fixed abrasive may be used in order to prevent dishing and enhance flatness of the face. After completion of primary polishing, the semiconductor substrate is transported by the

fourth robot 134 to the first cleaning unit 115 where it is cleaned. This cleaning is scrub-cleaning in which rolls having substantially the same length as the diameter of the semiconductor substrate are placed on the face and the backside of the semiconductor substrate, and the semiconductor substrate and the rolls are rotated, while pure water or deionized water is flowed, thereby performing cleaning of the semiconductor substrate.

After completion of the primary cleaning, the semiconductor substrate is transported by the fourth robot 134 to the second polishing apparatus 122 where the barrier layer 5 on the semiconductor substrate is polished. At this time, desired abrasive grains or the like are used, but fixed abrasive may be used in order to prevent dishing and enhance flatness of the face. After completion of secondary polishing, the semiconductor substrate is transported by the fourth robot 134 again to the first cleaning unit 115 where scrub-cleaning is performed. After completion of cleaning, the semiconductor substrate is transported by the fourth robot 134 to the second substrate reversing device 144 where the semiconductor substrate is reversed to cause the plated surface to be directed upward, and then the semiconductor substrate is placed on the substrate temporary placing table 145 by the third robot.

The semiconductor substrate is transported by the second robot 132 from the substrate temporary placing table 145 to the cap plating unit 117 where nickel-boron plating (cap plating), for example, is applied onto the surface of the interconnects 8 for the purpose of preventing oxidation of copper due to the atmosphere. The semiconductor substrate, in which the protective film 9 (see

FIG. 1C) has been formed on the surface of the interconnects 8 by the cap plating to protect the interconnects 8, is transferred by the second robot 132 to the third film thickness measuring device 146 where the thickness of the copper film is measured. Thereafter, the semiconductor substrate is transferred by the first robot 131 to the second cleaning unit 118 where the substrate is cleaned with pure water or deionized water. The cleaned semiconductor substrate is returned to the cassette 120a in the loading/unloading unit 120.

Example

Holes having a size of ϕ 0.5 μm x 0.5 μm depth (aspect ratio : 1.0) were formed at a predetermined pitch in the insulating film. After filling the holes with copper, the surface was flattened by a CMP treatment to prepare a sample (semiconductor wafer) having a size of 3 cm x 4 cm (with 6-pattern formation). The sample was subjected to electroless plating at a bath load of 200 ml/chip using a plating liquid having the composition shown in the following table 1.

Table 1

$CoSO_4 \cdot 7H_2O$	28.1 g/L
L-tartaric acid	82.5 g/L
$(NH_4)_2SO_4$	39.6 g/L
DMAB	1.5 g/L
TMAH (27%)	455 ml/L
H_2WO_4	5.0 g/L
PH	9.0
Temperature	80℃

After the completion of electroless plating, the sample was washed and dried. When the sample was observed under an SEM, it was found that a plated Co-W-B film grew selectively in the pattern formation region. The growth rate of the plated film was about 100nm/min; and the plated film was analyzed as follows:

Co: about 98.4 at %, W: about 1.0 at %, B: about 0.6 at %

FIGS. 7A and 7B are diagrams of SEM photographs of the sample. As shown in the Figures, there is no formation of voids within the copper film 14 embedded in the hole 12 formed in the insulating layer 10. Further, only the surface of the copper film 14, i.e. the surface of interconnects, is covered with the protective film 16 of the plated Co-W-B film, without deposition of the Co-W-B film on the surface of the insulating film 10, indicating high selectively of the plating.

Comparative Example

The same sample as used in Example was prepared. The sample was first immersed in a solution of $PdCl_2$(0.005 g/L) + HCl(0.2 ml/L) at 25℃ for one minute to impart the palladium catalyst to the sample. Next, the palladium-imparted sample was immersed in a plating liquid at 90℃ having the composition shown in the following Table 2, and electroless plating was performed at a bath load of 200 ml/chip.

Table 2

$CoCl_2 \cdot 6H_2O$ (g/L)	30
$(NH_4)_2 \cdot WO_4$ (g/L)	10
$Na_3C_6H_5O_7 \cdot 2H_2O$ (g/L)	80
$NaH_2PO_2 \cdot H_2O$ (g/L)	20
PH	pH = 10 with NaOH

After the completion of electroless plating, the sample was washed and dried. When the sample was observed under an SEM, it was found that a plated Co-W-P film grew selectively in the pattern formation region. The grow rate of the plated film was about 70 nm/min; and the plated film was analyzed as follows:

Co: about 89 at %, W: about 5 at %, P: about 6 at %

FIGS. 8A and 8B are diagrams of SEM photographs of the sample. As shown in the Figures, a void V is formed within the copper film 14 embedded in the hole 12 formed in the insulating layer 10. Further, not only the surface of the copper film 14, i.e. the surface of interconnects, is covered with the protective film 16 of the plated Co-W-P alloy film, but the alloy film 16a is deposited also on the surface of the insulating film 10 around the hole 12, i.e. region of unnecessary protection, thus indicating poor selectively of the plating.

According to the present invention, as described hereinabove, the use as reducing agent of an alkylamine borane free from sodium makes it possible to apply an oxidizing current to e.g. copper, a copper alloy, silver, or a silver alloy to thereby avoid the need for imparting a palladium catalyst, thus enabling a direct electroless plating, and can prevent contamination of the

semiconductor device with an alkali metal. This can reduce the requisite process steps and increase the throughput, prevent the formation of voids in the interconnects, thereby enhancing the reliability, and avoid the increase in interconnect resistance caused by palladium diffusion.

Moreover, the use of a plating liquid containing an alkylamine borane as a reducing agent enables a selective plating only onto the interconnect region.